Amendments to the Claims:

1. (Currently Amended) A Universal Serial Bus device comprising:

a first processor configured as a Universal Serial Bus device to provide a first set of services to an external host; and

a second processor, coupled to said first processor as a Universal Serial Bus host and coupled to a Universal Serial Bus device connector suitable for connection to said external host, configured to provide a second set of services to said external host, and configured to pass service data bi-directionally between said first processor and said external host for said first set of services,

wherein said first processor is further configured to have a plurality of normally open logical service switches, wherein said first set of services are unavailable to said second processor during bus enumeration from said first processor to said second processor while inter-processor communication services continue between said first and second processors.

2. (Currently Amended) The Universal Serial Bus device of claim 1, wherein:

~~said first processor is further configured to have a plurality of normally open logical service switches, wherein said first set of services are unavailable to said second processor during bus enumeration from said first processor to said second processor, and~~ wherein at least one of said plurality of normally open logical service switches will close with respect to at least one of said first set of services in response to a request by said second processor.

3. (Canceled) ~~The Universal Serial Bus device of claim 1, further comprising a wireless transceiver.~~

4. (Canceled) ~~The Universal Serial Bus device of claim 1:~~

~~wherein said second processor is further configured to transmit a de-configuration request to said first processor in response to at least one of a physical disconnection of said external host and a service disconnect message from said external host, and wherein said first processor is further configured to cancel at least one service in response to said de-configuration request.~~

5. (Previously Presented) A Universal Serial Bus device comprising:

a first processor configured as a Universal Serial Bus device to provide a first set of services to an external host; and

a second processor, coupled to said first processor as a Universal Serial Bus host and coupled to a Universal Serial Bus device connector suitable for connection to said external host, configured to provide a second set of services to said external host, and configured to pass service data bi-directionally between said first processor and said external host for said first set of services,

wherein said second processor is further configured to respond to a set configuration request from said external host by comparing configuration sets of said first processor and said second processor, transmitting a set interface request to said first processor if said configuration sets are different, and transmitting a configuration request to said first processor if said configuration sets are identical.

6. (Original) A method of Universal Serial Bus enumeration by a Universal Serial Bus device having a first processor and a second processor comprising:

connecting a host to said Universal Serial Bus device;

receiving, from said host, a set configuration request;

determining that said first processor and said second processor have the same configuration sets;

transmitting, by said second processor, a set configuration request to said first processor for the configuration of said second processor; and

closing, by said first processor, a logical switch to connect services to said second processor in response to said configuration request.

7. (Original) A method of Universal Serial Bus enumeration by a Universal Serial Bus device having a first processor and a second processor comprising:

connecting a host to said Universal Serial Bus device;

receiving from said host a set configuration request;

determining that said first processor and said second processor have different configuration sets;

transmitting by said second processor at least one set interface request to said first processor; and

closing, by said first processor, at least one logical switch to connect at least one service to said second processor in response to said at least one set interface request.